Attorney Docket No.: YOR920030258US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s):	W. Rhee et al.
Docket No.:	YOR920030258US1
Serial No.:	10/697,751
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Group:	2816
Examiner:	Linh M. Nguyen

Title:	Voltage-Controlled Delay Circuit Using Second-Order Phase Interpolation

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AMENDED APPEAL BRIEF

Commissioner for Patents
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Sir:

This Amended Appeal Brief is submitted in response to the Notice of Non-Compliant Appeal Brief dated May 15, 2007.

Appellants hereby appeal the current rejection of claims 1-15 of the above-referenced application.

REAL PARTY IN INTEREST

The present application is assigned to International Business Machines Corp., as evidenced by an assignment recorded February 5, 2004 in the U.S. Patent and Trademark Office at Reel 14309, Frame 759. The assignee, International Business Machines Corp., is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and interferences.

STATUS OF CLAIMS

Claims 1-15 are pending in the present application. Claims 1-6 and 9-14 stand rejected under 35 U.S.C. §102(b). Claim 15 stands rejected under 35 U.S.C. §102(b). Claims 7 and 8 stand rejected under 35 U.S.C. §103(a). Claims 1-15 are appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites a voltage-controlled delay line, comprising: a delay element; and a phase interpolation circuit coupled to the delay element; wherein the delay element and the phase interpolation circuit are operative to: (i) obtain an input signal and a complement of the input signal; and (ii) use the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal. The present specification provides an illustrative embodiment of the elements of claim 1 at page 4, line 26 through page 6, line 3.

More particularly, FIG. 3A illustrates a voltage-controlled delay line using second-order phase interpolation. Voltage-controlled delay line 300 includes a delay line (DLY) 302 (an example of the claimed delay element). Coupled to delay line 302 is a phase interpolation circuit (an example of the claimed phase interpolation circuit coupled to the delay element). The phase interpolation circuit includes a first weighting unit 304 for introducing weight α, a second weighting unit 306 for introducing weight β, a first summer 308, a third weighting unit 310 for introducing weight α, a second summer 312, a fourth weighting unit 314 for introducing weight α, a fifth weighting unit 316 for introducing weight β, a third summer 318, and a sixth weighting unit 320 for introducing weight β. An input signal (Vin) and a complement of the input signal are obtained.

As shown in FIG. 3A, voltage-controlled delay line 300 implements a second-order phase interpolation topology, where (as claimed) the input signal and the complement of the input signal are used to perform a phase interpolation process so as to realize a complete delay tuning range with

respect to the input signal. For example, an input signal (Vin) is weighted (α) by unit 304, and also delayed by delay line 302 (to generate signal Vin') and weighted (β) by unit 306. The respective outputs of units 304 and 306 are summed by summer 308 to generate signal V1. The output of summer 308 is weighted (α) by unit 310. Also, the output of delay line 302 is weighted (α) by unit 314. The complement of the input signal is weighted (β) by unit 316. The respective outputs of units 314 and 316 are summed by summer 318 to generate signal V2. The output of summer 318 is weighted (β) by unit 320. The respective outputs of units 310 and 320 are summed by summer 312. The output of summer 312 is the output signal (Vout) of voltage-controlled delay line 300. The tuning range associated with the VCDL 300 is illustrated in FIG. 3B. (Specification, page 4, line 26 through page 6, line 3).

Thus, advantageously, principles of the present invention provide a phase interpolation technique for voltage-controlled delay line (VCDL) implementation. The techniques of the invention employ a second-order phase interpolation topology to improve tuning range performance of the VCDL over process and temperature variation, wherein a complementary input signal is used to set an absolute 180-degree phase reference. As a result, the maximum (complete or full) tuning range of 180 degrees can be achieved regardless of internal delay variation. Such techniques may be employed in various circuits and systems, e.g., a delay-locked loop (DLL) circuit or a clock-and-data recovery (CDR) system.

Independent claim 7 recites a delay-locked loop circuit having all the elements of above-described claim 1, as well as an additional element of a phase detector coupled to the voltage-controlled delay line for generating an error signal for adjusting a phase shift associated with the voltage-controlled delay line. The present specification provides an illustrative embodiment of the elements of claim 7 at page 2, line 22 through page 3, line 1. More particularly, as depicted in FIG. 1A, a delay-locked loop (DLL) circuit 100 includes a voltage-controlled delay line (VCDL) 102 and a phase detector (PD) 104. PD 104 compares the timing difference between a reference clock edge and a clock edge from VCDL 102. PD 104 also generates an error voltage for VCDL 102 to adjust

the phase shift (i.e., control voltage Vctr fed back to VCDL 102). (Specification, page 2, line 22 through page 3, line 1).

Independent claim 8, having similar elements to the above-described claim 1, also recites a clock and data recovery system, comprising the additional elements of a clock recovery circuit for recovering a clock signal and a data recovery circuit coupled to the voltage-controlled delay line for recovering data in accordance with a clock signal received from the voltage-controlled delay line. The present specification provides an illustrative embodiment of the elements of claim 8 at page 3, lines 5-14. More particularly, as shown in FIG. 1B, variable delay circuit 110 includes a clock recovery circuit 112 and a data recovery circuit 116. This variable delay circuit may be used in clock-and-data recovery (CDR) systems, in which a clock (CLK) and data (Dout) are recovered from a single high-speed serial stream of non-return-to-zero (NRZ) data.

Independent claim 9 is a method claim having steps of above-described claim 1. Thus, the same sections of the present specification illustrated above in the mapping of claim 1 apply here for claim 9. More particularly, support for claim 9 is shown in FIG. 3A and page 4, line 26 through page 6, line 3.

Independent claim 15 is an apparatus claim having elements of above-described claim 1. The apparatus comprises a processor and memory arrangement. The voltage-controlled delay line described above may be implemented in accordance with a processor for controlling and performing the various operations as illustrated above in the mapping of claim 1, a memory, and an input/output interface. (Specification, page 7, lines 20-22).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(1) Claims 1-6 and 9-14 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,122,336 to Anderson (hereinafter "Anderson").

(2) Claim 15 is rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,133,773 to Garlepp et al. (hereinafter "Garlepp").

(3) Claims 7 and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Anderson in view of U.S. Patent No. 6,295,328 to Kim et al. (hereinafter "Kim").

ARGUMENT

(1) Claims 1-6 and 9-14 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,122,336 to Anderson (hereinafter "Anderson").

With regard to the issue of whether claims 1-6 and 9-14 are anticipated under 35 U.S.C. §102(b) by Anderson, the final Office Action contends that Anderson discloses all of the claim limitations recited in the subject claims. Appellants respectfully assert that Anderson fails to teach or suggest all of the limitations in claims 1-6 and 9-14, for at least the reasons presented below.

It is well-established law that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Appellants assert that the rejection based on Anderson does not meet this basic legal requirement, as will be explained below.

The present invention, for example, as recited in independent claim 1, recites a voltage-controlled delay line, comprising a delay element, and a phase interpolation circuit coupled to the delay element, wherein the delay element and the phase interpolation circuit are operative to: (i) obtain an input signal and a complement of the input signal; and (ii) use the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal. Independent claim 9 recites similar limitations.

Furthermore, as illustratively explained in the present specification at page 1, lines 15-23:

> Principles of the present invention provide a phase interpolation technique for voltage-controlled delay line (VCDL) implementation. The techniques of the invention may employ a second-order phase interpolation topology to improve tuning range performance of the VCDL over process and temperature variation. In one aspect of the invention, <u>the technique may use a complementary input signal to set an absolute 180-degree phase reference</u>. As a result, <u>the maximum (complete or full) tuning range of 180 degrees can be achieved</u> regardless of internal delay variation. Such techniques may be employed in various circuits and systems, e.g., a delay-locked loop (DLL) circuit or a clock-and-data recovery (CDR) system. (Underlining added for emphasis)

Thus, as recited in independent claims 1 and 9, the delay element and the phase interpolation circuit are operative to use the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal.

Anderson, as disclosed at column 3, lines 1-5, increases resolution of its frequency synthesizer by using interpolation to increase the number of clock phases. FIG. 4 of Anderson shows a ring oscillator 400 and phase interpolation unit 402. However, despite the assertion in the final Office Action, Anderson does not disclose a delay element and a phase interpolation circuit operative to use the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal, as recited in independent claims 1 and 9.

First, Anderson does not disclose use of the input signal and the complement of the input signal to perform a phase interpolation process. The Examiner points to signals $A\phi_0$ and $A\phi_4$ in FIG. 4 of Anderson, however, these are not the input signal and the complement of the input signal. As explained at column 4, lines 2-4, these signals are merely clock phases generated by the ring oscillator and sent to the phase interpolation unit.

Appellants respectfully point out that the present final Office Action was issued to change the Examiner's rationale for rejection from the previous final Office Action dated April 11, 2005. The only apparent change that was made was that the Examiner now considers $A\phi_4$ to be the complement of the input signal, rather than $A\phi_1$. However, for at least the reason given above (i.e., that signals $A\phi_0$ through $A\phi_7$ are merely clock phases generated by the ring oscillator and sent to the phase interpolation unit), the change in rationale does not remedy the deficiencies of the rejection.

Second, Anderson merely increases resolution of the frequency synthesizer by adding more clock phases. Anderson clearly does not provide a complete delay tuning range with respect to the input signal, as recited in independent claims 1 and 9. As defined in the present specification (page 1, lines 15-23), a complete delay tuning range with respect to the input signal is a tuning range of 180 degrees.

For at least these reasons, Appellants assert that independent claims 1 and 9, and the claims that depend therefrom, are patentable over Anderson.

In the final Office Action, in a section referred to as "Remarks and Conclusion," the Examiner again states his position that signals $A\phi_0$ and $A\phi_4$ in FIG. 4 of Anderson are the input signal and the complement of the input signal and that a complete delay tuning range is achieved therewith. However, for the reasons given above, Appellants respectfully disagree.

Furthermore, Appellants assert that the claims that depend from claims 1 and 9, namely, claims 2-6 and claims 10-14, are patentable over Anderson not only for the above reasons that claims 1 and 9 are patentable, but also because such dependent claims recite patentable subject matter in their own right.

In rejecting the dependent features, the final Office Action either generally cites FIG. 4 of Anderson or gives no specific reference to Anderson at all.

With regard to claims 2 and 10, the final Office Action states that FIG. 4 of Anderson discloses that the phase interpolation process is a second-order phase interpolation process. However, this does not appear to be the case.

With regard to claims 3 and 11, the final Office Action states that FIG. 4 of Anderson discloses that the delay tuning range is equivalent to 180 degrees of a period of the input signal. Again, as explained above, no where does Anderson teach or suggest a delay tuning range equivalent to 180 degrees of a period of the input signal.

With regard to claims 4 and 12, the final Office Action merely states that Anderson discloses that the delay tuning range is guaranteed over a process variation without giving any specific referential support. Anderson appears to disclose no such feature.

With regard to claims 5 and 13, the final Office Action merely states that Anderson discloses that the delay tuning range is guaranteed over a temperature variation without giving any specific referential support. Again, Anderson appears to disclose no such feature.

With regard to claims 6 and 14, the final Office Action states that FIG. 4 of Anderson discloses that the complement of the input signal is used to generate an absolute 180-degree phase

reference. Again, as explained above, no where does Anderson teach or suggest that the complement of the input signal is used to generate an absolute 180-degree phase reference.

(2) Claim 15 is rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,133,773 to Garlepp et al. (hereinafter "Garlepp").

Regarding claim 15, the final Office Action asserts that Garlepp discloses all the limitations in said claim. Appellants assert that the rejection based on Garlepp does not meet the basic legal requirement of the above-cited Federal Circuit decision in *Verdegaal Bros. v. Union Oil Co. of California*, as will be explained below.

While Garlepp, at column 4, lines 36-43, discloses a phase interpolator circuit which provides tunability of phase interpolation performance, Garlepp clearly does not disclose using the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal, as recited in independent claim 15.

The phase interpolator tunability disclosed by Garlepp is realized via controllable capacitive loading, as clearly stated at column 4, line 37 and 38, of Garlepp. That is, Garlepp does not use the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal, as recited in independent claim 15. In fact, while Garlepp mentions an extended range for its adjustable phase interpolator (column 3, lines 31-34), Garlepp makes no mention of a realization of a complete delay tuning range with respect to the input signal, as in the claimed invention. As defined in the present specification (page 1, lines 15-23), a complete delay tuning range with respect to the input signal is a tuning range of 180 degrees.

For at least these reasons, Appellant assert that independent claim 15 is patentable over Garlepp.

In the final Office Action, in the section referred to as "Remarks and Conclusion," the Examiner again states his position that Garlepp discloses a complete delay tuning range in

accordance with the input signal and the complement of the input signal. However, for the reasons given above, Appellants respectfully disagree.

(3) Claims 7 and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Anderson in view of U.S. Patent No. 6,295,328 to Kim et al. (hereinafter "Kim").

Regarding the §103(a) rejection of claims 7 and 8 based on the combination of Anderson and Kim, Applicants assert that such claims are patentable over the combination due at least to the above-mentioned deficiencies in Anderson. That is, claim 7 recites using the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal, and claim 8 recites using the clock signal and the complement of the clock signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the clock signal. Based at least on the remarks above with respect to Anderson in terms of claims 1 and 9, it is clear that Anderson fails to disclose these limitations. Thus, the Anderson/Kim combination is deficient.

Appellants also assert that the combination of Anderson and Kim is improper since the final Office Action fails to provide sufficient rationale for the motivation to combine the two references.

For at least these reasons, Appellants assert that independent claims 7 and 8 are patentable over the Anderson/Kim combination.

In view of the above, Appellants believe that claims 1-15 are in condition for allowance, and respectfully request withdrawal of the §102(b) and §103(a) rejections.

Respectfully submitted,

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APPENDIX

1. A voltage-controlled delay line, comprising:

a delay element; and

a phase interpolation circuit coupled to the delay element;

wherein the delay element and the phase interpolation circuit are operative to: (i) obtain an input signal and a complement of the input signal; and (ii) use the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal.

2. The voltage-controlled delay line of claim 1, wherein the phase interpolation process is a second-order phase interpolation process.

3. The voltage-controlled delay line of claim 1, wherein the delay tuning range is equivalent to 180 degrees of a period of the input signal.

4. The voltage-controlled delay line of claim 1, wherein the delay tuning range is guaranteed over a process variation.

5. The voltage-controlled delay line of claim 1, wherein the delay tuning range is guaranteed over a temperature variation.

6. The voltage-controlled delay line of claim 1, wherein the complement of the input signal is used to generate an absolute 180-degree phase reference.

7. A delay-locked loop circuit, comprising:

a voltage-controlled delay line comprising: (i) a delay element; and (ii) a phase interpolation circuit coupled to the delay element; wherein the delay element and the phase interpolation circuit are operative to obtain an input signal and a complement of the input signal; and use the input signal

and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal; and

a phase detector coupled to the voltage-controlled delay line for generating an error signal for adjusting a phase shift associated with the voltage-controlled delay line.

8. A clock and data recovery system, comprising:

a clock recovery circuit for recovering a clock signal;

a voltage-controlled delay line, coupled to the clock recovery circuit, comprising: (i) a delay element; and (ii) a phase interpolation circuit coupled to the delay element; wherein the delay element and the phase interpolation circuit are operative to obtain the clock signal and a complement of the clock signal; and use the clock signal and the complement of the clock signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the clock signal; and

a data recovery circuit coupled to the voltage-controlled delay line for recovering data in accordance with a clock signal received from the voltage-controlled delay line.

9. A method for delaying an input signal, comprising the steps of:

obtaining an input signal and a complement of the input signal; and

using the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal.

10. The method of claim 9, wherein the phase interpolation process is a second-order phase interpolation process.

11. The method of claim 9, wherein the delay tuning range is equivalent to 180 degrees of a period of the input signal.

12. The method of claim 9, wherein the delay tuning range is guaranteed over a process variation.

13. The method of claim 9, wherein the delay tuning range is guaranteed over a temperature variation.

14. The method of claim 9, wherein the complement of the input signal is used to generate an absolute 180-degree phase reference.

15. Apparatus for delaying an input signal, comprising:

a memory; and

at least one processor coupled to the memory and operative to: (i) obtain an input signal and a complement of the input signal; and (ii) use the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.